DESIGN OF MEMORY EFFICIENT VLSI ARCHITECTURE FOR REAL TIME MULTIMEDIA APPLICATION

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ABSTRACT: On-chip memory hierarchy for a video, contains the data memory and the context memory organizations for better optimization. Compressing the memory space is important in VLSI, in order to reduce the power consumption, power dissipation and area. HCC and LDO techniques are used to compress the on-chip memory space and thereby reduces the reconfiguration time and the data reference time. HCC, the contexts to be constructed in hierarchical fashion in order to eliminate repetitive portions of the contexts. In LDO, it increases the reuse ratio of memory space automatically and also for a several time references. The hierarchical storage & re usage for saving required memory space, without affecting the performance. In future by increasing the size of macro blocks from 8x8 into 64x64 in H.265 CODEC to achieve better compression rate and to increase throughput rate using pipelining technique.

Keywords: HCC, LDO, CODEC, On-chip memory, Macro blocks

I. INTRODUCTION
Multimedia technology, improved the quality of human lives from large device to portable devices, from home to outdoors, and from specific people to everybody. Digital video technology is considered to be the most important part of multimedia providing applications such as high definition TV, 3D graphics, digital cinema, camera, and so on. The multimedia system used to store and/or transmit video data becomes an essential concern. The key role of a video system to reduce the video data without losing any of its quality through an video CODEC(encoder and decoder),or known as video coding.

Video consumes 66% of the total Internet data flow, and that number continues to increase rapidly. Users want to watch high quality videos but, for an online video providers, costs of purchasing the network bandwidth and the storage devices grow increasingly every year. Compressing video reduces its file size, it is important, because smaller files upload faster and thus it save bandwidth and storage costs, and load quicker when it played back. Video is composed of a series of still frames normally 24-60 frames per second and only part of the image changes from frame to frame. Instead of storing two nearly-identical frames in a video file, only the parts of the image to be changed are recorded. For eg. If you have a friend waving to the camera, and your friend’s arm is the only thing moving in the shot, and thus the image information of your friend’s arm is the only thing recorded. The method a computer used for determining the amount of change between frames is called the codec.

For every couple of frames, the codec will pick a key frame that to be serves as a reference for all the frames after it. H.261 and H.263 are now widely used for real-time video communications in a network. H.264 is now a widely adopted standard and its an international standard for video compression. H.264 provides significant improvements in coding efficiency, latency, complexity and robustness. H.264 format is more broadly available in network cameras, video management and video encoders software, system designers and integrators will need to make sure that the products and vendors they choose and support this new open standard.

H.264 is a standard for video compression, and now it is currently one of the most commonly used format for recording, compression and distribution of high definition video. In this re usage
scheme and hierarchical storage are used to save memory space required, without affecting the performance.[1] In LDO, the on-chip data are classified into two types, based on the lifetime of data. The short-lifetime of data are stored in the FIFO to increase the reuse ratio of memory space automatically and can be used to pass the value from one stage to next. And RAM for storing the long lifetime data. In order to perform inter & intra prediction, the previous frames and blocks need to be stored for reference. A H.264 video encoder which carries out prediction, DCT transform and encoding processes to produce a compressed H.264 bit stream, H.264 video decoder carries out the complementary processes of decoding, inverse transform and reconstruction to produce a decoded video sequence. The HCC and LDO techniques used in H.264 CODEC uses the logic element of 6869, speed of 153.12MHZ and the dissipate power of 514.47 mw. And in proposed HEVC is said to double the data compression ratio compared to H.264 at the same level of video quality. And it can alternatively be used to provide improved video quality at the same bit rate. It can support 8K UHD and resolution up to 8192x4320.

I. SYSTEM DESIGN

Operation
The video is composed of series of still frames. DCT transform is performed to first frame of video after transformation it stored as reference in RAM and then the next frame is get processed for DCT and then the difference between the frames is get predicted by motion estimation i.e the reference between the different types of frame are realized by a process called motion estimation. Motion estimation used to estimates the residual value obtained from DCT and motion compensation predicts which prediction is performed to frames. The use of deblocking filter is to improve the visual quality and prediction performance by smoothening sharp edges between the macro block. IDCT is performed to recover the original frame. In this also HCC and LDO technique used in H.265 CODEC thereby achieving the reduction in area and dissipation of power and increases speed when compared to H.264.

II. DETAILED SYSTEM DESIGN

Context memory: The context memories store the contexts, and get accessed during the configuration. The context memory organization is crucial in the reconfigurable system, because affects the size of contexts and reflects the configuration.[1] The context size determines both the reconfiguration overhead and the silicon area. The smaller the contexts, and it smaller the memory space required for the contexts. Smaller the size of contexts assist in reducing the transfer delay of contexts from off-chip memory to on-chip memory. Overhead in the communication heavily depends on the context memory organization.
On-chip memory: On-chip memory is the simplest type of memory to use in an FPGA-based embedded system. And it provides the highest throughput, lowest latency memory to be possible in an FPGA-based embedded system. Advantage of on-chip memory requires no additional board space or circuit-board wiring because it is implemented directly on the FPGA. On-chip memory can also save development time and cost.

Motion estimation: The references between the different types of frames are realized by a process called motion compensation or motion estimation. The correlation in terms of motion between two frames is represented by a motion vector. The frame correlation and the pixel arithmetic difference is strongly depends on how the good estimation algorithm is implemented. Good estimation results in better quality of the coded video sequence and higher compression ratio.

Intra prediction: When a block or macro blocks is coded in intra mode, a prediction block is formed based on previously encoded and reconstructed blocks in the same frame. This prediction is subtracted from the current macro block or block and the result of the residual is compressed and transmitted to the decoder, together with the information required for the decoder to repeat the prediction process. The decoder creates an identical prediction and adds this to the decoded residual or block.

Inter prediction: It aims to remove temporal redundancies in a video sequence. Inter prediction macro blocks must reside in P-slices and require an history of previously encode frames and it to be kept in memory. The availability of multiple reference frames for motion compensation is a new feature in H.264/AVC standard. [9] For inter prediction a 16x16 macro block to be partitioned into any 4x4 multiple.

Hierarchical configuration context: In non-hierarchical, the context is stored repeatedly and it directly included in the task context. The main advantage of HCC is to compress the memory space required for the contexts. The context are get constructed in hierarchical fashion in order to completely eliminate the repetitive portions of the context and it can be accessed and located conveniently.

III. RESULTS & DISCUSSION

MODELSIM OUTPUT:

Fig 3 shows the simulation output waveform after processing the frames by performing DCT and prediction process.

AREA UTILIZATION REPORT: The flow summary depicts the successful compilation and execution. The
report gives register usage and memory storage of a system chip design.

Fig 4 the area can be calculated by knowing the total logic elements and register, memory bits and total pins.

**PERFORMANCE REPORT:**

![Performance Report](image)

**IV. COMPARISON RESULTS**

<table>
<thead>
<tr>
<th>TYPES USED</th>
<th>AREA</th>
<th>SPEED</th>
<th>POWER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Existing CODEC</td>
<td>6869</td>
<td>153.12MHZ</td>
<td>514.4 mW</td>
</tr>
<tr>
<td>Proposed CODEC</td>
<td>6037</td>
<td>147.73MHZ</td>
<td>477.8 mW</td>
</tr>
</tbody>
</table>

Table shows the trade off analyzes of Video codec with LDO and HCC methods with QUARTUS II hardware synthesis using STRATIX III family.

**V. CONCLUSION AND FUTURE WORK**

The proposed HCC and LDO techniques are used to compress the memory space and reduce the reconfiguration time using H.265 CODEC. The DCT block, FIFO and RAM for data references are designed thereby reducing On-Chip data memory size without affecting the performance of system and thereby achieving the area, power and performance than by using H.264. Future enhancements includes, modify DCT blocks, prediction blocks and to carried out pipelining for better throughput and performance
metric analyzes in H.265 and its FPGA implementations.

VI. REFERENCES


